10/049474
10049474 . 071802 Rec'd PCT/PTO 12 FEB 2002

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[10191/2235]

SEMICONDUCTOR ARRANGEMENT AND METHOD OF MANUFACTURE

Background Information

The present invention starts out from a semiconductor arrangement and a method for manufacturing the semiconductor arrangement according to the species defined in the independent claims. German Patent Application No. P 4320780.4 describes a semiconductor diode having a first layer made of two partial layers, and a second layer, where the second layer is situated on the first partial layer.

Summary of the Invention

In contrast, the present invention's semiconductor arrangement and method for manufacturing the semiconductor arrangement, which include the characterizing features of the independent claims, have the advantage of providing diodes having an increased maximum permissible power and less forward voltage, given a constant chip surface, in a manner suitable for large-scale mass production, without a large amount of additional engineering expense. This is particularly advantageous, when a maximum preselected chip surface area should not be exceeded in order to save chip surface, and when the size of the contact socket used to contact the semiconductor arrangement should not exceed a certain magnitude, in order to avoid paying for an increased current-carrying capacity of diodes particularly used in a motor-vehicle rectifier system, with an increased volume of the entire rectifier system. Therefore, the present invention shows how, given a constant surface area of the silicon chip, the allowable current load can be increased and the thermal loading of the silicon chip can be reduced in a manner whose technology can be realized relatively simply. In so doing, a reduction in the forward voltage is simultaneously achieved.

The effect of additional saw grooves proves to be particularly advantageous, because later, when the socket and lead wire are soldered to the diode chip, the grooves lead to a better, bubble-free soldering procedure (capillary effect), and the grooves filled with solder result in additional, more effective cooling of the chip, which extends into the depth of the silicon body and therefore thermally couples the chip to the heat sink in a more intensive manner.

Additional advantages result from the further refinements specified in the dependent claims, as well as from improvements to the semiconductor arrangement and method indicated in the independent claims.

Brief Description of the Drawing

Exemplary embodiments of the present invention are shown in the drawings and explained in detail in the following description.

The figures show:

Figure 1a	a cross-sectional side view of a diode;
Figure 1b	a plan view of a diode;
Figure 2	a method step; and
Figures 3 and 4	further method steps.

Description of the Exemplary Embodiments

Figure 1a shows a cross-sectional side view of a semiconductor chip 7, which is in the form of a diode. Chip 7 has a first semiconductor layer (2, 3, 4), which is made of a first partial layer 2, a second partial layer 3, and a third partial layer 4. The doping of n-doped partial layer 2 is on the order of 10^{18} cm^{-3}. Partial layer 3 is n-doped to a concentration of

approximately 10^{14} cm^{-3}, and partial layer 4 is doped to an - concentration of approximately 10^{20} cm^{-3}. Two trenches 10 are introduced into partial layer 2, which extend into partial layer 3. These trenches 10 are situated in inner region 13 of chip 7. Edge regions 12 of the chip have a bevel 11, which extends into partial layer 3 as do trenches 10. Deposited onto first partial layer 2, both into trenches 10 and in bevel 11, is a second layer 20, whose regions in trenches 10 and bevels 11 are designated as continuation regions 23 and further continuation regions 24 of second layer 20, respectively. Second layer 20 is p-doped and has a doping on the order of 10^{20} cm^{-3}. The wafer topside, which is covered by layer 20, and the wafer bottom side, which is formed by layer 4, are provided with metallic coatings 22 and 21, respectively. Figure 1b shows a plan view of the same component. The top of chip 7 is covered by metallic coating 22. As a result of the trenches 10 that are introduced, this metallic coating 22 has a pattern characterized by corresponding depressions.

The p-n junction region of the diode is formed by p-doped layer 20 and n-doped layers 2 and 3. As a result of the trenches 10 that are introduced, continuation regions 23 in interior 13 of chip 7 form a p-n junction with second partial layer 3. These regions lead to a reduction in the forward voltage of the diode, with metallic coating 22 being used as the anode and metallic coating 21 being used as the cathode. The four grooves in the interior of chip 7 (cf. Figure 1b) allow the electrical load to be increased by over 12% in comparison with an identically constructed diode not having grooves in the interior. In other words, a diode that can withstand, for example, a 65 A load may be converted to a diode having a maximum load of 75 A. An 80 A diode becomes a 90 A diode. The forward voltage may be reduced by approximately 60 mV (measured at a 100 A load). The four additional grooves or trenches in the interior of chip 7 also

result in the chip being soldered more effectively and free of bubbles, i.e. the socket and lead wire are attached to the diode chip in an improved manner. In addition, the grooves filled with solder during this soldering procedure (not shown in the figure) ensure that the chip cools in an improved manner, since the solder in the grooves, which then completely fills the grooves, thermally couples the chip in an intensive manner, to a metal base used as a heat sink.

Figure 1b represents the special case of a square chip 7. However, not only are squares possible, but also other surfaces that are defined by straight edges (e.g. a hexagon or an octagon) and have additional, corresponding, internal grooves parallel to the edges.

Figure 2 shows a semiconductor wafer having a first partial layer 2, a second partial layer 3, and a third partial layer 4. All three partial layers are n-doped. The starting point for manufacturing this sequence of layers is a weakly n-doped wafer, whose dopant concentration corresponds to the dopant concentration of partial layer 3. N-dopant, e.g. phosphorus, is then introduced onto and diffused into the topside and bottom side, using film diffusion. A layer, whose dopant concentration corresponds to partial layer 2, is consequently formed on the topside, and a layer, whose dopant concentration corresponds to partial layer 4, is formed on the bottom side. In this context, the dopant concentration of the layers is determined by the dopant concentration of the films.

The manufacture of such a layer sequence is already known from German Patent Application No. P 4320780.4. As an alternative, this sequence of layers can also be manufactured using neutral films, as is described in the German patent application having the number 19857243.3.

Figure 3 shows a further step of the manufacturing method according to the present invention. In this context, trenches 10 are introduced into the semiconductor wafer, which subdivide partial layer 2 into subsections, trenches 10 extending through to partial layer 3. Trenches 10 can be introduced, for example, by sawing or etching them. The spacing of trenches 10 is adjusted in such a manner, that the wafer can subsequently be separated along the trenches, into individual chips; after the separation, each chip still having at least one trench 10 in its interior. However, the wafer surface is first cleaned prior to being processed further, in order to remove any possibly remaining particles from the surface.

In comparison with German Patent Application P 4320780.4, the spacing of the saw lines is halved during the sawing-in procedure (in order to obtain two additional grooves per chip) or reduced to one third (in order to obtain four additional grooves per chip). In this case, the spacing of the grooves is typically 1-3 mm. No additional method step is necessary here, since, as is known from P 4320780.4, the sawing-in procedure is executed to lay out the chip edge, anyway. One must only set the line spacing to be somewhat smaller during the sawing-in procedure. This does not considerably change the processing time of this sawing step, since the wafer handling, the alignment, and the cleaning with deionized water done in the automatic sawing device after the sawing-in procedure, are carried out anyway.

After the introduction of trenches 10, a p-dopant such as Boron is introduced into the topside. At the same time, the dopant concentration of bottom layer 4 can be increased if this appears to be advantageous. P-dopant is introduced again, using film diffusion. In this diffusion step, possible defects present in the silicon monocrystal in the immediate vicinity

of trenches 10 are repaired. The p-diffusion converts the top layer of the silicon wafer into a p-conductive region. The thickness of this p-layer is approximately uniform over the surface, even in the trenches. In Figure 4, the resulting p-conductive layer is represented by reference numeral 20. Subsequent to the deposition of layer 20 and the possible intensification of the doping of partial layer 4, the two sides of the wafer are metallized so that p-conductive layer 20 is provided with a metallic coating 22 and n-doped, third partial layer 4 is provided with a metallic coating 21. In a further step, the wafer is diced along separation lines 25, into a plurality of individual diodes, so that individual chips 7 are formed whose structure is described in Figures 1a and 1b. Prior to sawing the wafer along separation lines 25, the wafer side having metallic coating 21, i.e. the bottom side, is pasted to a sawing sheet so that the individual chips do not fly off in an uncontrolled manner or become damaged.

The width of the saw lines during the sawing-in procedure is approximately 40 to 150 μm, and the lengths of the chip edges are in the range of approximately 5 mm. The area of the additional saw grooves in the interior of the individual chips only makes up a few percent of the chip surface. Of course, the method of the present invention can also be used to manufacture diodes doped in an opposite manner, i.e. diodes where a p-doped wafer is used as a starting point, in place of an n-doped wafer.